Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) A branch predictor comprising:

a branch prediction generator for generating a predicted conditional branch of a branch instruction;

a comparator for generating a comparison signal by comparing the predicted conditional branch from the branch prediction generator with a real conditional branch of the branch instruction;

an accuracy history table for storing an accuracy history of the predicted conditional branch;

a first state transition logic circuit for generating accuracy history bits to be stored to the accuracy history table in response to the comparison signal; and

a multiplexer having a first input and a second input for receiving the predicted conditional branch and an inverted version of the predicted ~~condition~~ conditional branch, respectively, for selecting one of the predicted conditional branch and the inverted predicted conditional branch, and for the selected one of the predicted conditional branch and the inverted predicted conditional branch as a final branch prediction outcome based on a state of a single selection input of the multiplexer; wherein

a single predicted accuracy history signal is applied to the single selection input of the multiplexer to select one of the predicted conditional branch and the inverted predicted conditional branch, the predicted accuracy history signal being a single most significant bit of the accuracy history bits and being directly applied to the single selection input of the multiplexer, such that the single accuracy history signal selects between the predicted conditional branch and the inverted predicted conditional branch to be output as the final branch prediction outcome.

2. (Original) The branch predictor according to claim 1, wherein the branch prediction means comprises:

a branch history register for storing conditional branches of previous branch instructions;

a pattern history table for storing pattern history bits used for generating the predicted conditional branch corresponding to the conditional branches of the previous branch instructions stored in the branch history register; and

a second state transition logic circuit for generating the pattern history bits in response to the real conditional branch of the branch instruction.

3. (Original) The branch predictor according to claim 2, wherein the second state transition logic circuit includes an up/down saturating counter.

4. (Canceled)

5. (Original) The branch predictor according to claim 1, wherein the comparator generates the comparison signal having a first logic value when the predicted conditional branch is the same as the real conditional branch, and generates the comparison signal having a second logic value when the predicted conditional branch is different from the real conditional branch.

6. (Original) The branch predictor according to claim 1, wherein the first state transition logic circuit includes an up/down saturating counter.

7. (Original) The branch predictor according to claim 6, wherein the first state transition logic circuit is used after learning the predicted branch accuracy of patterns of previous branch instructions.

8. (Canceled)